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**Alexandria University**

**Faculty of Engineering**

**Electronics and Communications Engineering Program**

**2023-2024**

Full Custom Design of

**4-Bit Ripple Carry Adder**

**VLSI - EEC 433**

Spring 2024

By Student:

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**Electronics and Communications Engineering**

**Alexandria University**

A computer screen shot of a computer

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A graph with red and blue lines

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A graph of a function

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Inverter Characteristic Curve

A screenshot of a computer

Description automatically generated

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**3**

**1**

**1**

**1**

**1**

**2**

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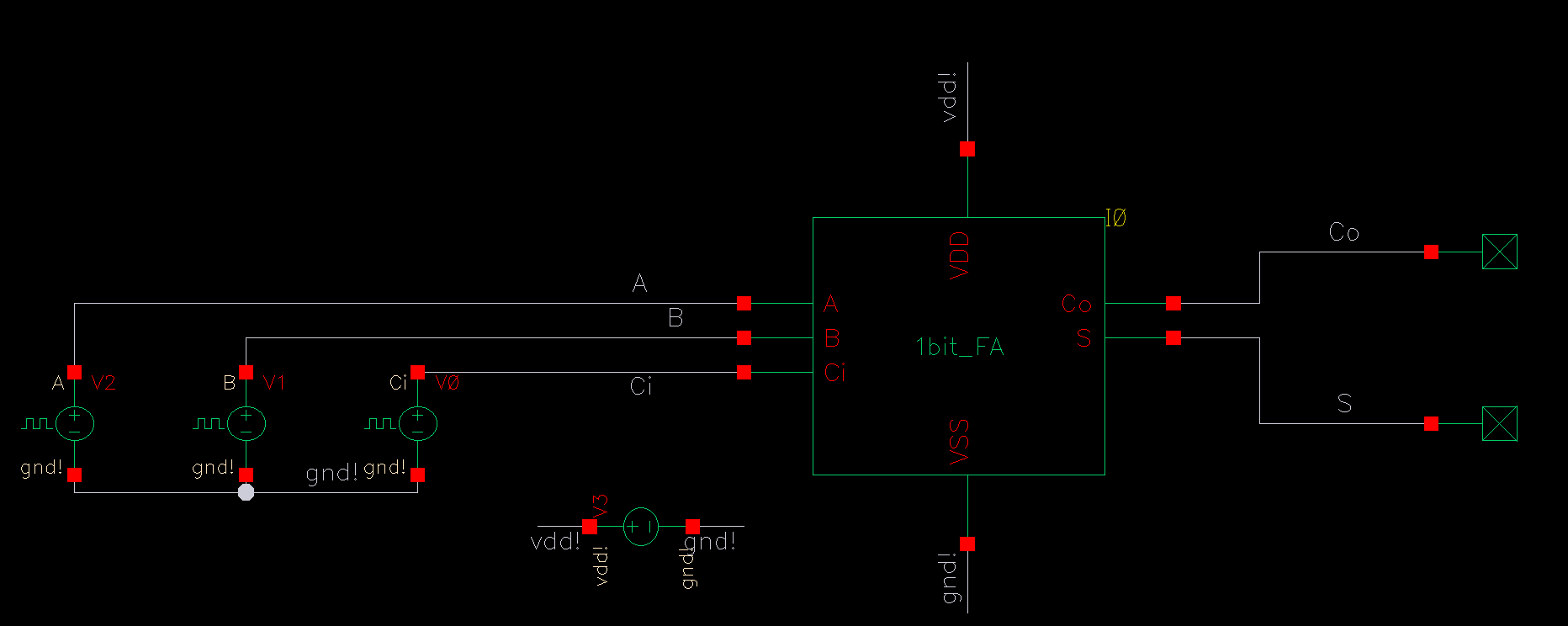
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Full Adder Circuit Schematic



1 bit Full Adder symbol and Test bench

A screenshot of a computer

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Ci

B

A

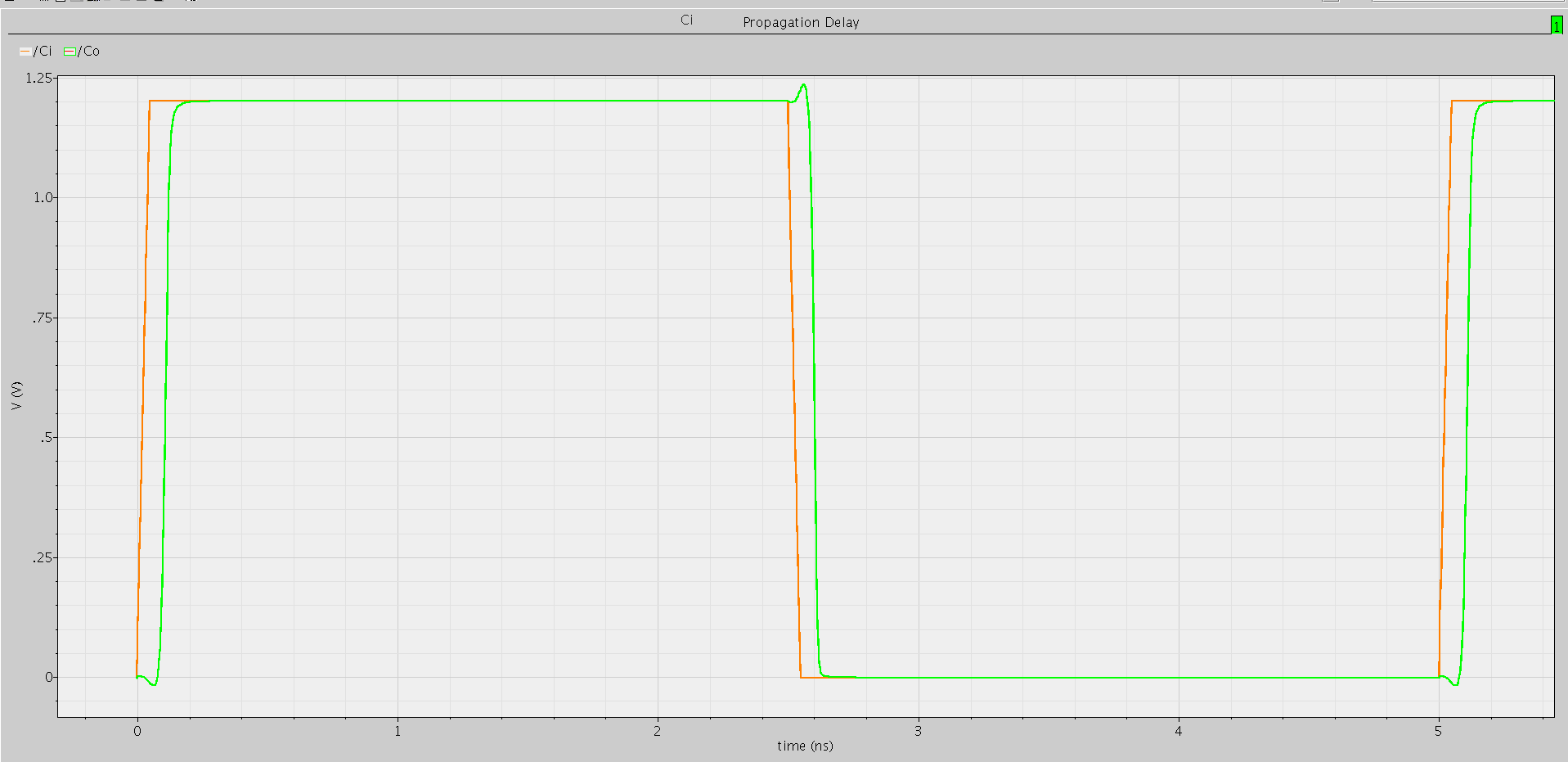
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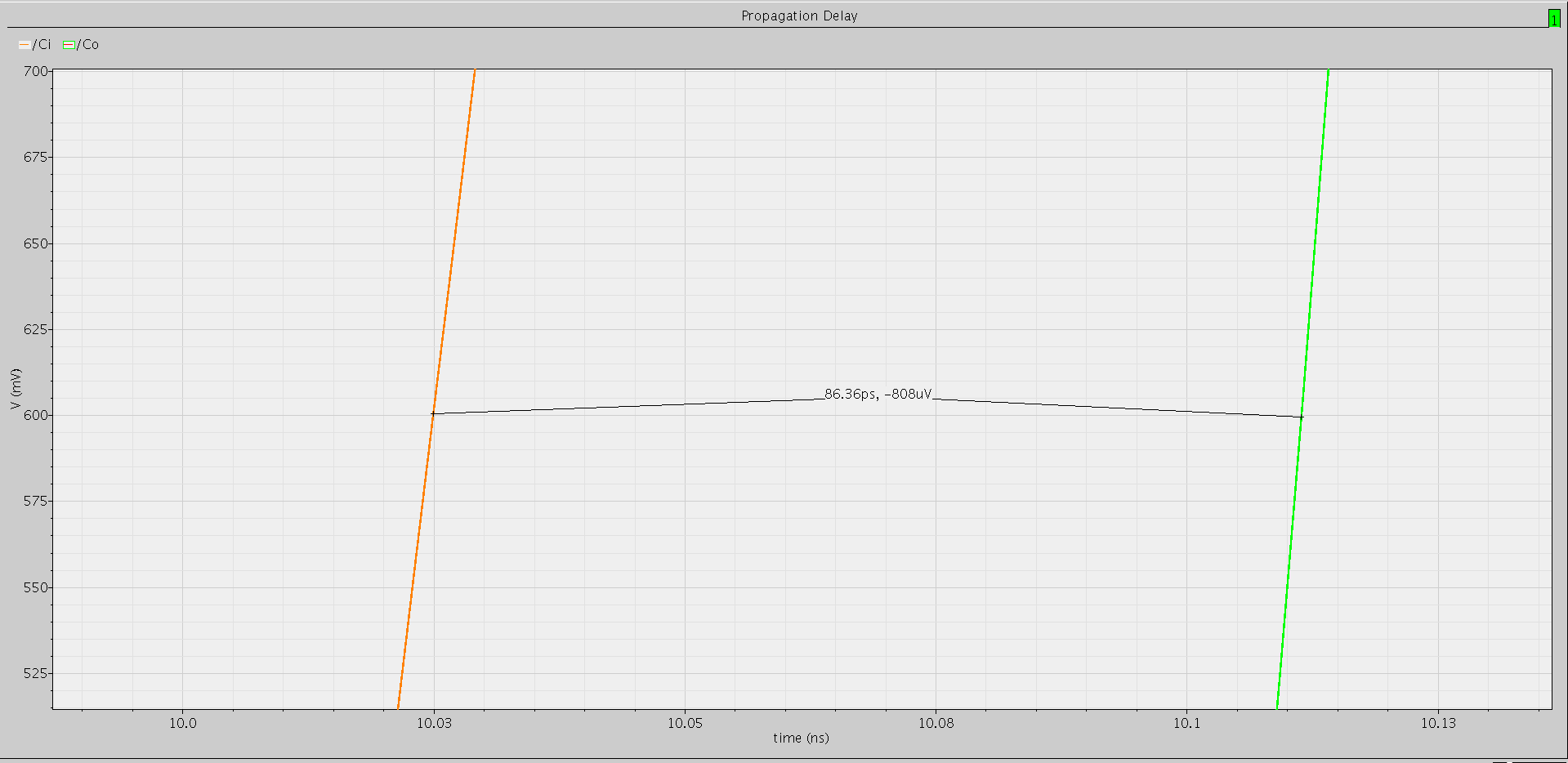
Co

Verifying the Functionality of the Full Adder Circuit



Propagation delay for single 1-bit full adder without load = 86.64 pS







Power Consumption = 15.5 uW

A screenshot of a video game

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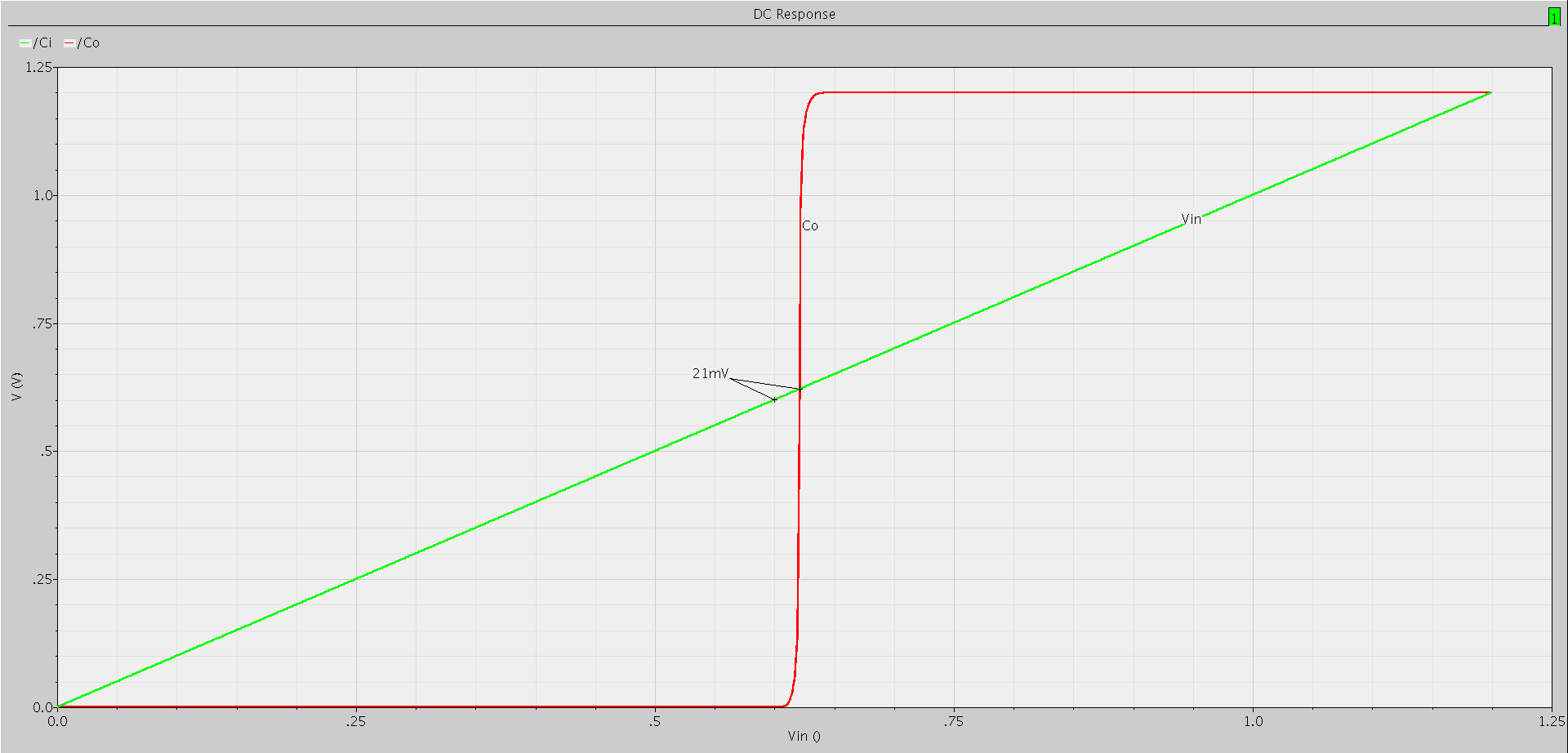
Test bench schematic for calculating the propagation delay with 1 FA Load



Propagation delay for one loaded 1-bit FA = 139.2 pS

A screen shot of a graph

Description automatically generated



DC Transfer Characteristics, Changing “Cin” from 0 to 1.2 V linearly and monitoring “Co”.

The mid point is 620 mV, we can redesign for closer point to 600 mV.

A screenshot of a computer

Description automatically generated

Circuit Test Bench, with Ideal 4-bit Carry Adder to verify the output of the designed Circuit

A screen shot of a graph

Description automatically generated

Ideal and Practical “Co” signals

A graph with red and green lines

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Ideal and Practical “S0” signals

A screenshot of a graph

Description automatically generated

Ideal and Practical “S1” signals

A screen shot of a graph

Description automatically generated

Ideal and Practical “S2” signals

A screenshot of a graph

Description automatically generated

Ideal and Practical “S3” signals

Now we have verified the functionality of the 4-bit ripple carry adder designed circuit.

A computer screen shot of a computer

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We have set Ci to 500 MHz clock while A = 0101 , B = 1010, so as to mirror the input carry to the output carry.  

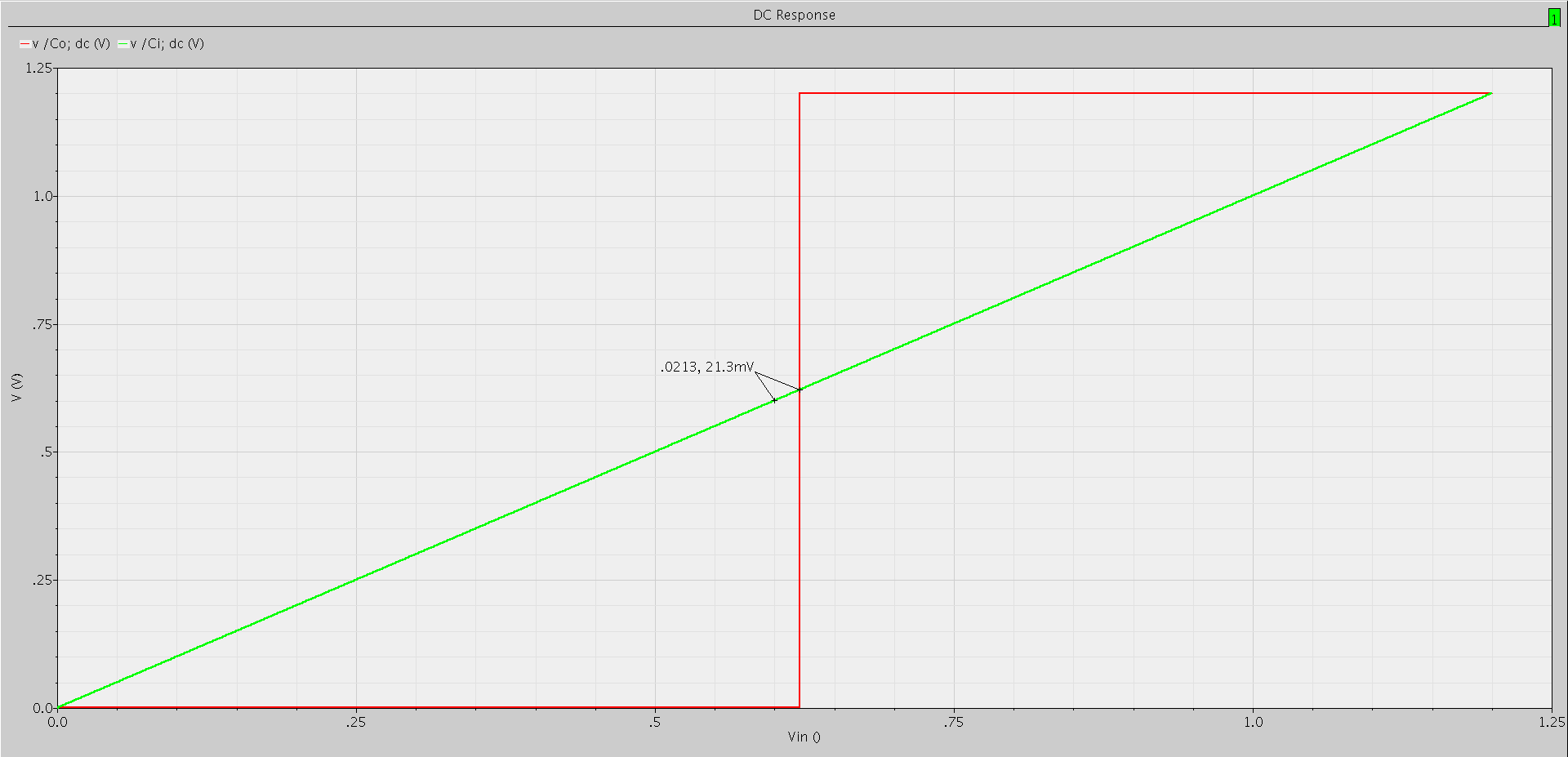

Propagation Delay of the 4-bit ripple adder between Ci and Co of the final stage = 662.5 pS

A graph on a white sheet

Description automatically generated

 500 MHz output Carry

Approximate Power Consumption at 500 MHz Switching 



Input/Output Transfer Characteristics for Ci to Co

**CONCLUSION**

**Transistor Sizing for a single bit FA:**

- 2 Inverters each one with PMOS (1105n/130n) and NMOS (250n/130n)

- 3 Stacked PMOS transistors with (3\*1105n/130n)

- 3 Stacked NMOS transistors with (3\*250n/130n)

- 9 transistors for the rest of PUN (Pull Up Network) with (2\*1105n/130n)

- 9 transistors for the rest of PDN (Pull Down Network) with (2\*250n/130n)

With total number of 28 Transistors for a single cell.

**Area Estimation:**

PMOS: (9\*2 + 3\*3 + 2\*1) \* 1105n \* 130n = 4.1658 um2 without routing

NMOS: (9\*2 + 3\*3 + 2\*1) \* 250n \* 130n = 0.9425 um2 without routing

Approximate area could be = 1.5 \* (4.1658 + 0.9425) = 7.6625 um2 for a single 1 bit FA

Total approximate area = 4 \* 7.6625 = 30.65 um2

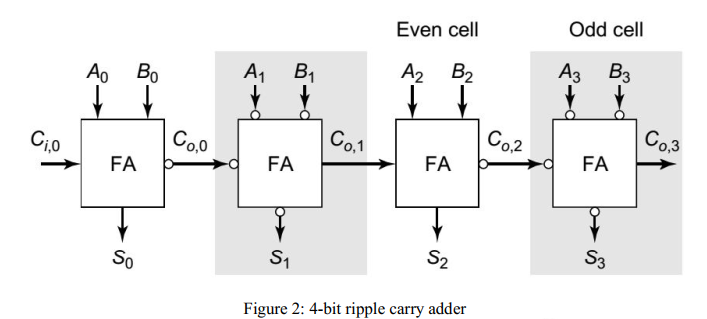
**Propagation Delay: 662.5 pS**

**Power Consumption: 373.2 uW**

**Technology: 130 nm (min Length), 150 nm (min Width)**

Following We will exploit the inverting property where “Inverting all the inputs of a full-adder cell also inverts all the outputs”. This should exclude the extra inverters we added in the odd cells.







|  |  |
| --- | --- |
| Inverter Symbol | Inverter Schematic |
|  |  |

Wp = 1105n, Wn = 250n

A computer screen shot of a circuit board

Description automatically generated

New Schematic for the single FA cell with inverted outputs without extra inverters

A screenshot of a computer

Description automatically generated

The Connections of the inverters, reducing the total inverter count by two and reducing the inverters at the critical path by 4.

A computer screen shot of a circuit board

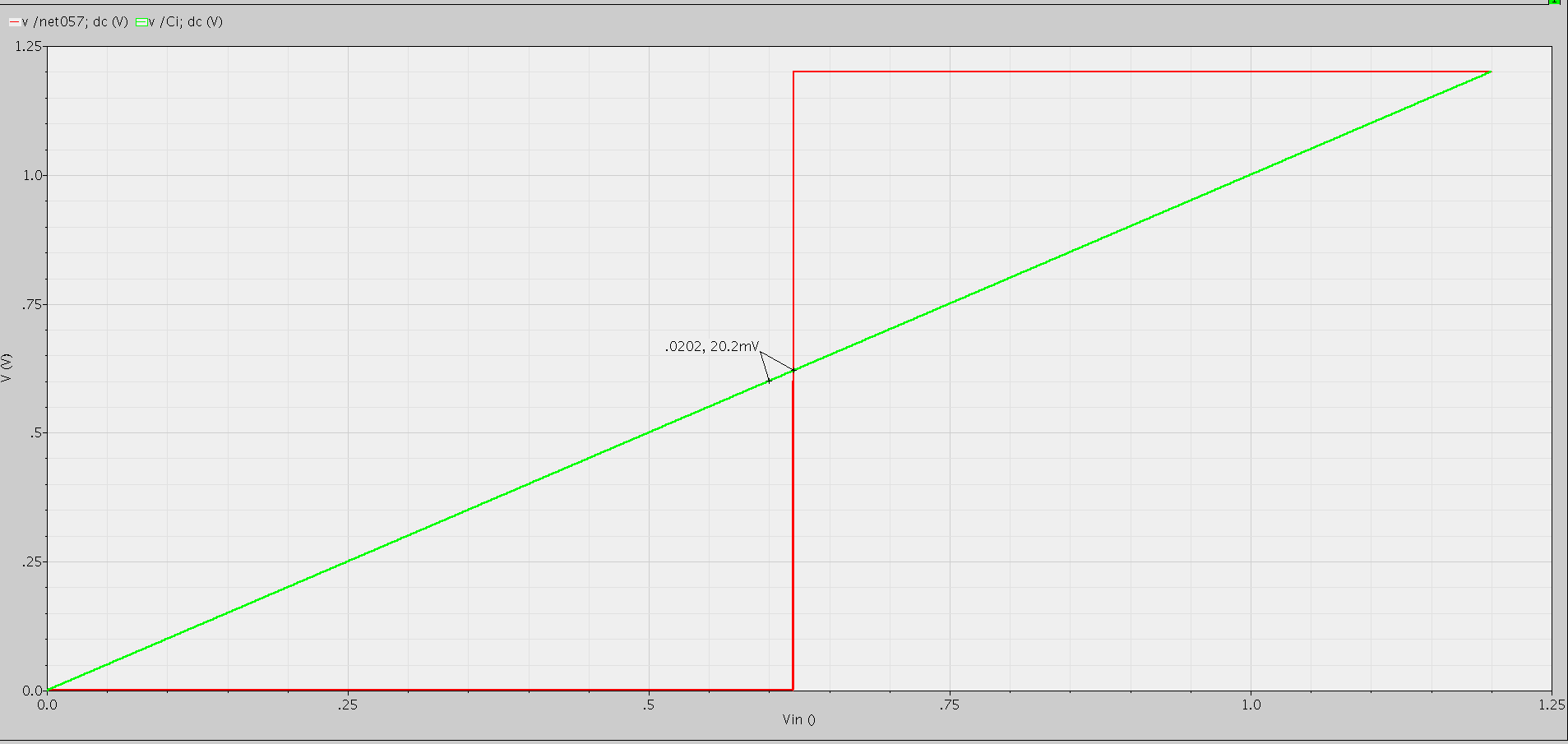
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The New Design Test Bench

A graph with red and green lines

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Ideal and Practical “Co” signals



Voltage Transfer Characteristics

A screenshot of a computer

Description automatically generated

Ideal and Practical “S0” signals

A screenshot of a graph

Description automatically generated

Ideal and Practical “S1” signals

A screen shot of a graph

Description automatically generated

Ideal and Practical “S2” signals

A graph with red and green lines

Description automatically generated

Ideal and Practical “S3” signals



Power consumption for the second design = 304.2 uW

A graph showing a graph of a graph

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The delay Difference between the two designs of 4-bit ripple carry adder = 138.3 pS

A graph of a graph

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The propagation delay of the second design = 526.17 pS

**CONCLUSION**

**Transistor Sizing for a single bit FA:**

- 3 Stacked PMOS transistors with (3\*1105n/130n)

- 3 Stacked NMOS transistors with (3\*250n/130n)

- 9 transistors for the rest of PUN (Pull Up Network) with (2\*1105n/130n)

- 9 transistors for the rest of PDN (Pull Down Network) with (2\*250n/130n)

With total number of 24 Transistors for a single cell.

In addition to another 6 Inverters for connections each one with PMOS (1105n/130n) and NMOS (250n/130n)

**Area Estimation:**

PMOS: (9\*2 + 3\*3 ) \* 1105n \* 130n = 3.87855 um2 without routing

NMOS: (9\*2 + 3\*3 ) \* 250n \* 130n = 0.8775 um2 without routing

Approximate area could be = 1.5 \* (3.87855 + 0.8775) = 7.134 um2 for a single 1 bit FA

Total approximate area = 4 \* 7.134 + 6\*(1.105+0.250)\*0.130\*1.5= 30.12 um2

**Propagation Delay: 526.17 pS**

**Power Consumption: 304.2 uW**

**Technology: 130 nm (min Length), 150 nm (min Width)**